WHEC
WEIHAI HUALING OPTO-ELECTRONICS CO., LTD

Notice: This is not a final specification.
Some parameters are subject to change

PL6R310SDC-XXXXX

Approved by customer		

A.20.5.7 original

1. Description

This specification is applied to PL6R310SDC- XXXXX Contact Image Sensor module with an analog parts of PL6R310S- XXXXX,an image processing control board(CL27).

2. Outline

Item		Specification	Note
Scanning width		310 mm	
Sensor element density		600 DPI	
Effective number of sensor elements		7322 elements 12# to 7333# (Full:7344elements)	
Scanning speed	Color	10KHz	
	B & W	30KHz	
Data speed (Camera Link)		595MHz	7×85MHz
Rod lens array		Two rows	L16
Light source		Red λp = 630nm ± 15nm Green λp = 520nm ± 15nm Blue λp = 465nm ± 10nm	
Power supply		+5V × 3 A **T.B.D**	
LED Power		+24.0V × 1A	
Analog data output		Block#1 432 pixels …… Block#17 432 pixels	Synchronous
Digital data output		Camera Link Interface	
Command communication		Serial Interface	
Read Position		14.8mm	
Dimensions		Figure 1	

3. Description of Interface

Pin No.	I/O	Signal	Pin No.	I/O	Signal	Function
1	-	GND	14	I	GND	
2	O	TxOUT0-	15	O	TxOUT0+	Data from Camera Link Transmitter
3	O	TxOUT1-	16	O	TxOUT1+	Data from Camera Link Transmitter
4	O	TxOUT2-	17	O	TxOUT2+	Data from Camera Link Transmitter
5	O	TxCLK_OUT-	18	O	TxCLK_OUT+	Clock from Camera Link Transmitter
6	O	TxOUT3-	19	O	TxOUT3+	Data from Camera Link Transmitter
7	I	SerTC(RxD)+	20	I	SerTC(RxD)-	Seria Communication Data Transmit
8	O	SerTFG(TxD)-	21	O	SerTFG(TxD)+	Seria Communication Data Receive
9	I	CC1-	22	I	CC1+	TRIG Signal
10	I	CC2+	23	I	CC2-	Not Used
11	I	CC3-	24	I	CC3+	Not Used
12	I	CC4+	25	I	CC4-	Not Used
13	I	GND	26	-	GND	Grand

4. Camera Link Interface

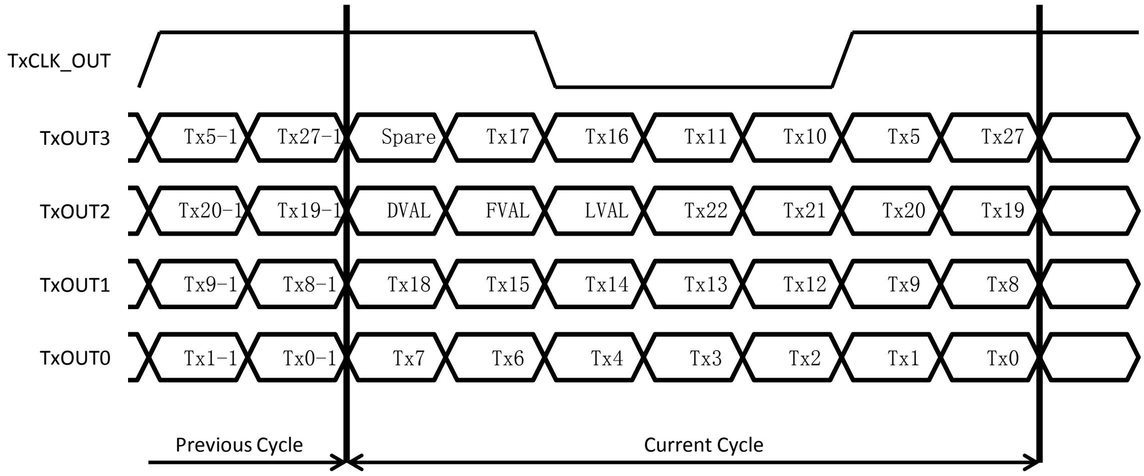


Fig 4-1 Camera Link Data Format

bit	RGB	bit	RGB
TX_0	R[0]	TX_14	G[5]
TX_1	R[1]	TX_15	B[0]
TX_2	R[2]	TX_16	B[6]
TX_3	R[3]	TX_17	B[7]
TX_4	R[4]	TX_18	B[1]
TX_5	R[7]	TX_19	B[2]
TX_6	R[5]	TX_20	B[3]
TX_7	G[0]	TX_21	B[4]
TX_8	G[1]	TX_22	B[5]
TX_9	G[2]	TX_23	Spare
TX_10	G[6]	TX_24	LVAL
TX_11	G[7]	TX_25	FVAL
TX_12	G[3]	TX_26	DVAL
TX_13	G[4]	TX_27	R[6]

Table4-1 Camera Link Bit Assignment

5. Serial Interface

This serial interface using SerTC and SerTFG to transfer command data.

5.1 Serial interface protocol

This serial interface uses the ASCII code.

	Value
Baud rate	115200
Start bit	1
Data bit	8
Parity bit	none
Stop bit	1
Flow control	none
Board⇒CIS	SerTC
CIS⇒Board	SerTFG

Table6-1 Serial interface protocol

5.2 Command Format

Command	Contents								
	1	2	3	4	5	6	7	8	9
CB Register read	r	r	SP	Addr_Hi	Addr_Lo	SP	SP	SP	CR
CB Register write	r	w	SP	Addr_Hi	Addr_Lo	SP	Data_Hi	Data_Lo	CR
Camera Link Register read	m	r	SP	Addr_Hi	Addr_Lo	SP	SP	SP	CR
Camera Link Register write	m	w	SP	Addr_Hi	Addr_Lo	SP	Data_Hi	Data_Lo	CR
Correction start	s	v	SP	SP	SP	SP	SP	SP	CR
Scan start	v	p	SP	SP	SP	SP	SP	SP	CR
Scan stop	s	p	SP	SP	SP	SP	SP	SP	CR
Reset	r	e	SP	SP	SP	SP	SP	SP	CR
Raw data mode	t	h	SP	o	n	SP	SP	SP	CR
Correction data mode	t	h	SP	o	f	SP	SP	SP	CR

Table6-2 Command Format

5.3 Response Format

Response	Contents							
	1	2	3	4	5	6	7	8
Error reply	〉	0	0	0	0	0	0	0
Command reply	〉	0	K	CR	〉	0	0	0
Register read reply	〉	0	K	SP	Data_Hi	Data_Lo	CR	〉
Correction reply	〉	S	V	SP	0	K	CR	〉

Table6-3 Response Format

Table5-3 Response Format

6.List of Register

＜Register Map 1＞

①These are registers in CB-Board.
②These register values are read from EEPROM during initialization processing. (At start, the reset is released)
③While stand-by mode (READY = High), these register values can be re-write by the serial interface.
④These register values are written to EEPROM by execution of the Correction processing.
⑤These register values can be read by the serial interface.
⑥Read command is 'rr', and Write command is 'rw'.

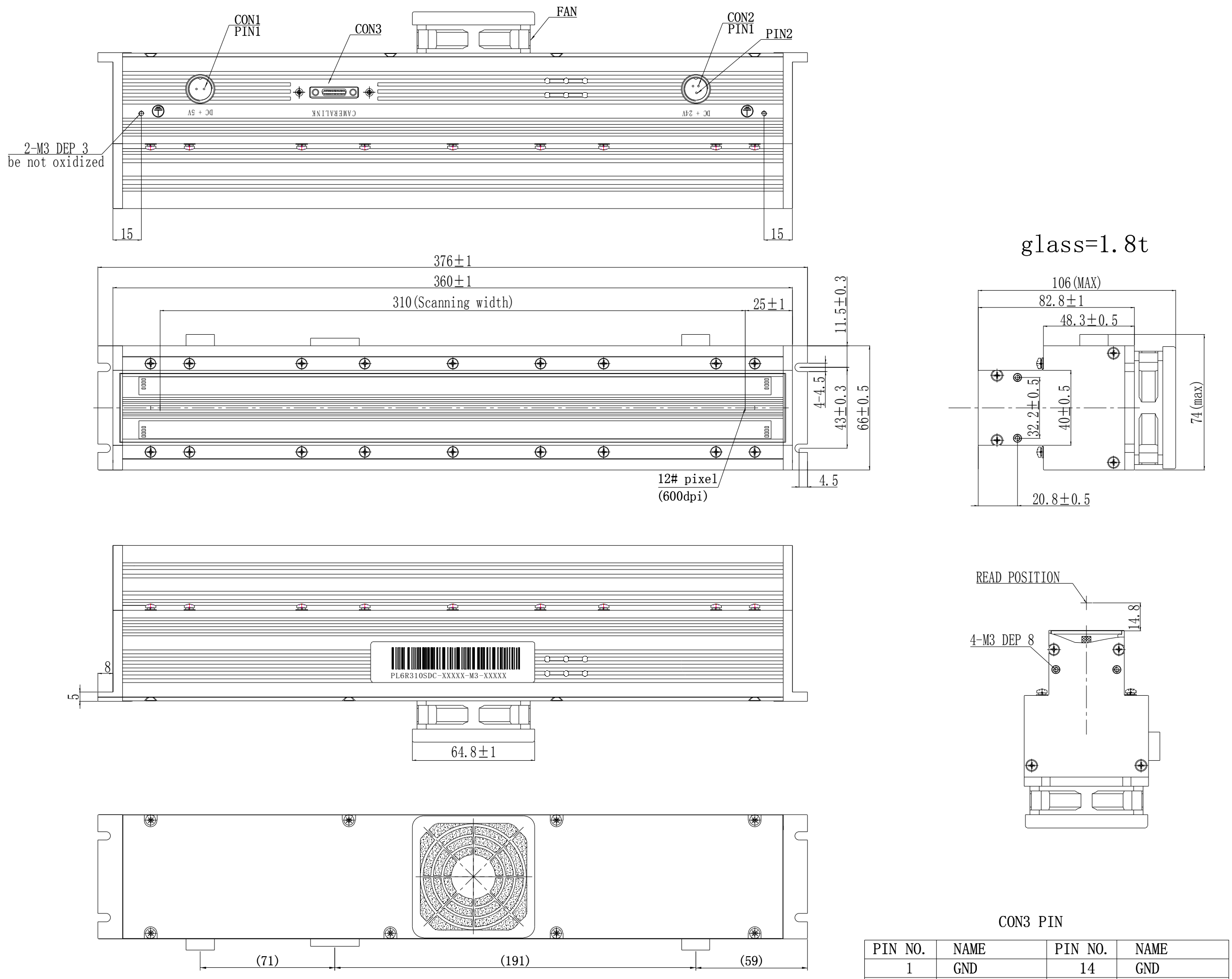
Item	Function	Name	Address [7:0]	Data 7	6	5	4	3	2	1	0	Default	Explanation
FPGA	LED setting cycle1	LEDcyc1	80	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	1000_0000	・This register is setting of LED ON/OFF 1:ON 0:OFF ・80h-87h is LED setting of cycle 1-8. ・When 0h is set, its cycle becomes invalid. ・Only 1 cycle, the mixed-LED setting is possible. The mixed-LED : Some LEDs light up simultaneous at 1 cycle. Simultaneous setting is below 4 colors. ・The same LED setting is prohibited.
	LED setting cycle2	LEDcyc2	81	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0100_0000	
	LED setting cycle3	LEDcyc3	82	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0010_0000	
	LED setting cycle4	LEDcyc4	83	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0000_0000	
	LED setting cycle5	LEDcyc5	84	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0000_0000	
	LED setting cycle6	LEDcyc6	85	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0000_0000	
	LED setting cycle7	LEDcyc7	86	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0000_0000	
	LED setting cycle8	LEDcyc8	87	R	G	B	IR	Add-A	Add-B	Add-C	Add-D	0000_0000	
	Various setting1	CONF1	88	CNT Set1	Color INH	Dark INH	Duty INH	CNT Set0	LED Lighting Setting	N/A	Auto AGC Setting	0000_1100	bit2:LED Lighting setting :0= one side 1= both sides bit7,3:CNT set:0=100dpi series, 1=600dpi series, 2=1200dpi series bit6,5,4,0:Correction Option 0=ON 1=OFF bit6=White Correction, bit5=Dark Correction, bit4=LED Duty, bit0=Auto Gain
	Various setting2	CONF2	89	N/A	N/A	Chip Setting[1:0]		CDS2delay[3:0]				0000_0000	bit3-0:Latch timming setting with CDSCLK2 and CISCLK 0=16/16、1-15=n/16 bit5,4:Chip Setting 0=2-1-1, 1=1-1-2, 2=4-0-0
	Total Pixel (Lower)	ALLELM_LO	90	D7	D6	D5	D4	D3	D2	D1	D0	7344	This register is the value of total sensor elements Set the value by a binary number in D12-D0. (The maximum 23328)
	Total Pixel (Upper)	ALLELM_UP	91	N/A	D14	D13	D12	D11	D10	D9	D8		
	Effective Pixel (Lower)	EFFELM_LO	92	D7	D6	D5	D4	D3	D2	D1	D0	7322	This register is the value of effecttive sensor elements Set the value by a binary number in D12-D0. (The maximum 23328)
	Effective Pixel (Upper)	EFFELM_UP	93	N/A	D14	D13	D12	D11	D10	D9	D8		
	Start Pixel (Lower)	STRPIX_LO	94	D7	D6	D5	D4	D3	D2	D1	D0	12	This register is the start pixel number of the effective sensor elements. Set the value by a binary number in D12-D0. (The maximum 23328)
	Start Pixel (Upper)	STRPIX_UP	95	N/A	D14	D13	D12	D11	D10	D9	D8		
	The value of invalid clk	INVLCLK	96	D7	D6	D5	D4	D3	D2	D1	D0	82	This register is the dummy output (from SI to Pixel#1 output) clock number. Set the value by a binary number in D7-D0. The value is [Pixel#1 appearance clock number] - 1
	Pixel Density	DPISEL	97	N/A	N/A	N/A	N/A	N/A	D2	D1	D0	4	Set the value of sensor element density 101:1200DPI、100:600DPI、011:300DPI、010:200DPI、 001:100DPI、000:50DPI
	LED-ON start position (Lighting up prohibited period)	LED_START	98	D7	D6	D5	D4	D3	D2	D1	D0	82	Set the number of LED-ON starting clocks. Set the value by a binary number in D7-D0. Basically, set the same value as the dummy output clock number
	Output selection	OUTSEL	99	N/A	N/A	N/A	N/A	N/A	OUTSEL[2:0]			0	Output digital data selection 0: White & Black correction, 1: White correction, 2: Black correction, 3:The coefficient of the white correction, 4: Dark data, 5: No correction (6-7: White & Black correction)
	Dummy Line Number	DUM_LINE	9C	N/A	N/A	N/A	N/A	N/A	D2	D1	D0	0	Empty feed number of lines setting 0:0, 1:50, 2:100, 3:200, 4:400, 5:600, 6:800, 7:1000
	Correction target value R	TARG_V_R	B0	D7	D6	D5	D4	D3	D2	D1	D0	217	Setting of the correction target value. Set the value every each color. * D7-D0: target value (Binary number)
	Correction target value G	TARG_V_G	B1	D7	D6	D5	D4	D3	D2	D1	D0	217	
	Correction target value B	TARG_V_B	B2	D7	D6	D5	D4	D3	D2	D1	D0	217	
	Correction target value IR	TARG_V_IR	B3	D7	D6	D5	D4	D3	D2	D1	D0	217	
	Correction target value Add-A	TARG_V_A	B4	D7	D6	D5	D4	D3	D2	D1	D0	217	
	Correction target value Add-B	TARG_V_B	B5	D7	D6	D5	D4	D3	D2	D1	D0	217	
	Correction target value Add-C	TARG_V_C	B6	D7	D6	D5	D4	D3	D2	D1	D0	217	
	Correction target value Add-D	TARG_V_D	B7	D7	D6	D5	D4	D3	D2	D1	D0	217	

＜Register Map 2＞

①These are registers in Camera-Link-Board.
②These register values are NOT written to EEPROM. So these register values are set 00h at power off.
③These register values can be read and written by the serial interface.
④Read command is 'mr', and Write command is 'mw'.

Item	Function	Name	Address [7:0]	Data 7	6	5	4	3	2	1	0	Default	Explanation
FPGA	AFE Clock Speed	J_AFECLK	00	N/A	N/A	D5	D4	D3	D2	D1	D0	11000	Set the value of AFE clock speed 18h=24MHz, 24h=36MHz, 30h=48MHz, Other=Don't set
	Trigger Mode	J_TRIGSEL	02	N/A	N/A	N/A	N/A	SYNC	N/A	WAITTIM	INSEL	10	INSEL:Start timming Mode 0=Internal, 1=External WAITTIM:Wait time 0=0s, 1=3s SYNC:Triger timming 0=Internal, 1=External
	Camera Link Data Format	J_CLD	03	N/A	N/A	N/A	N/A	N/A	N/A	D1	D0	0	D[1:0]:0=RGB, 1=mono 3color, 2=mono 3TAP, 3=mono 1color(red)

Figure 1. Dimensions



1. CONNECTOR:
   CON1:16M-2F
   CON2:16M-3F
   CON3:12226-8250-00PL
2. CIS TYPE AND LOT NUMBER ARE PRINTED
   ON THE BOTTOM OF THE SENSOR FRAME.
   PL6R310SDC-XXXXX - M 3 - XXXXX
   (CIS TYPE) (2019)(Mar.)(SERIES No.)

Year	10	11	12	13	14	15	16	17	18	19	20
	A	B	D	E	F	H	J	K	L	M	N
Year	21	22	23	24	25	26	27	28	29	30	31
	O	P	R	S	T	U	V	W	X	Y	Z

Month	10	11	12
	A	B	D

CON1 PIN

PIN NO.	NAME
1	5V
2	GND

CON2 PIN

PIN NO.	NAME
1	24V
2	GND
3	NC
4	NC

CON3 PIN

PIN NO.	NAME	PIN NO.	NAME
1	GND	14	GND
2	TxOUT0-	15	TxOUT0+
3	TxOUT1-	16	TxOUT1+
4	TxOUT2-	17	TxOUT2+
5	TxCLK_OUT0-	18	TxCLK_OUT0+
6	TxOUT3-	19	TxOUT3+
7	SerTC+	20	SerTC-
8	SerTFG-	21	SerTFG+
9	CC1-	22	CC1+
10	CC2+	23	CC2-
11	CC3-	24	CC3+
12	CC4+	25	CC4-
13	GND	26	GND